

The
United
States
of
America



The Commissioner of
Patents and Trademarks

Has received an application for a patent for a new and useful invention. The title and description of the invention are enclosed. The requirements of law have been complied with, and it has been determined that a patent on the invention shall be granted under the law.

Therefore, this

United States Patent

Grants to the person(s) having title to this patent the right to exclude others from making, using, offering for sale, or selling the invention throughout the United States of America or importing the invention into the United States of America for the term set forth below, subject to the payment of maintenance fees as provided by law.

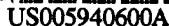
If this application was filed prior to June 8, 1995, the term of this patent is the longer of seventeen years from the date of grant of this patent or twenty years from the earliest effective U.S. filing date of the application, subject to any statutory extension.

If this application was filed on or after June 8, 1995, the term of this patent is twenty years from the U.S. filing date, subject to any statutory extension. If the application contains a specific reference to an earlier filed application or applications under 35 U.S.C. 120, 121 or 365(c), the term of the patent is twenty years from the date on which the earliest application was filed, subject to any statutory extension.

J. Todd Johnson

Acting Commissioner of Patents and Trademarks

Ollie M. Person
Attest



Staats et al.

[45] **Date of Patent:** **Aug. 17, 1999**

- ISO/IEC 13213 ANSI/IEEE Standard 1212, "Information Technology — Microprocessor Systems — Control and Status Registers (CSR) Architecture For Microprocessor Buses". First Edition, pp. 1-125, (Oct. 5, 1994).**

Primary Examiner—Glenn A. Auve
Assistant Examiner—Eric S. Thlang
Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman

A computer system consists of a plurality of nodes, each with an associated local host, coupled together with a plurality of point-to-point links. An isochronous data channel is established within the computer system between a first subset of the plurality of nodes. The isochronous data channel includes a linked list of buffers which are used as temporary storage locations for data transmitted on the isochronous data channel. Each node which is part of the isochronous data channel is configured as a sender or a receiver and data transmissions are commenced. The presence of isochronous data in the channel generates an interrupt which signals a central processing unit (CPU) that data is available. The data is transferred to an associated location within the linked list of buffers and the CPU then moves on to other tasks. In other embodiments, data is transferred using DMA techniques rather than interrupt driven events. Buffers can also be used to transmit isochronous data.

11 Claims, 4 Drawing Sheets

